

## **Claims**

1. A test structure for use in DRAM comprising:

a semiconductor substrate;

a transistor formed on said semiconductor substrate, said transistor comprising a first region and a second region, both said first region and said second region being formed in said semiconductor substrate, said first region and said second region for use as source/drain regions of said transistor;

a deep trench capacitor formed in said semiconductor substrate and adjacent to said transistor, said deep trench capacitor having a first width;

a shallow trench insulator (STI) formed in a top portion of said deep trench capacitor, said STI having a second width, wherein said second width is substantially shorter than said first width;

a third region formed in said semiconductor substrate and adjacent to said deep trench capacitor;

a first contact formed on said semiconductor substrate and contacting with said first region; and

a second contact formed on said semiconductor substrate and contacting with said third region.

2. The test structure of Claim 1, wherein said semiconductor substrate is a silicon substrate.

3. The test structure of Claim 1, wherein said transistor comprises a gate, said gate comprises a silicon oxide layer formed on said semiconductor substrate and an electric conductor layer formed on said silicon oxide layer.

4. The test structure of Claim 1, further comprising two gate contacts formed on said semiconductor substrate and located on said deep trench capacitor.

5. The test structure of Claim 4, wherein said gate contact comprising a silicon oxide layer formed on said semiconductor substrate and an electric conductor layer formed on said silicon oxide layer.
6. The test structure of Claim 3 or 5, wherein said electric conductor layer is a metal silicide layer.
7. The test structure of Claim 1, wherein said first region, said second region and said third region are formed by doping a dopant into said semiconductor substrate.
8. A test structure for use in DRAM comprising:
  - a silicon substrate;
  - a transistor formed on said silicon substrate, said transistor comprising a first region and a second region, both said first region and said second region being formed in said silicon substrate, said first region and said second region for use as source/drain regions of said transistor;
  - a deep trench capacitor formed in said silicon substrate and adjacent to said transistor, said deep trench capacitor having a first width;
  - a shallow trench insulator (STI) formed in a top portion of said deep trench capacitor, said STI having a second width, and said second width being substantially shorter than said first width;
  - two gate contacts formed on said silicon substrate and located on said deep trench capacitor, and said two gate contacts being separated by said STI;
  - a buried strap formed in said silicon substrate and adjacent to said deep trench capacitor;
  - a first contact formed on said silicon substrate and contacting with said first region;
  - and
  - a second contact formed on said silicon substrate and contacting with said buried

strap.

9. The test structure of Claim 8, wherein said transistor comprises a gate, said gate comprises a silicon oxide layer formed on said silicon substrate and an electric conductor layer formed on said silicon oxide layer.
10. The test structure of Claim 8, wherein said gate contact comprising a silicon oxide layer formed on said silicon substrate and an electric conductor layer formed on said silicon oxide layer.
11. The test structure of Claim 9 or 10, wherein said electric conductor layer is a metal silicide layer.